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U.S. UTILITY Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10061475	02/01/2002	257		2811	Loke

**APPLICANTS: Krutsick Thomas;

**CONTINUING DATA VERIFIED:
none
Loke

** FOREIGN APPLICATIONS VERIFIED:
none
Loke

PG-PUB DO NOT PUBLISH ☐ | RESCIND ☐

Foreign priority claimed ☐ yes ☑ no
35 USC 119 conditions met ☐ yes ☑ no
Verified and Acknowledged Examiners's intials Loke

ATTORNEY DOCKET NO 10

TITLE : Method of fabricating complementary self-aligned bipolar transistors

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G.
ISSUE FEE: Amount Due / Date Paid		DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER	Primary Examiner / PREPARED FOR ISSUE	Application Examiner

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